Claims

[c1] What is claimed is:

1. An electrostatic discharge protection circuit, comprising:

a first bipolar transistor coupled between a first circuit node and a second circuit node, said first bipolar transistor having a non-uniform subcollector region geometry, said first bipolar transistor having a different value for collector to emitter breakdown voltage than a value for collector to emitter breakdown voltage of an otherwise identical bipolar transistor having a uniform subcollector region geometry.

[c2] 2. The circuit of claim 1, wherein said different value for collector to emitter breakdown voltage than a value for collector to emitter breakdown voltage of an otherwise identical bipolar transistor having a uniform subcollector region geometry is a higher value.

[c3] 3. The circuit of claim 1, wherein said first bipolar transistor has a different value for unity current gain cutoff frequency than a value for unity current gain cutoff frequency of said otherwise identical bipolar transistor.

[c4] 4. The circuit of claim 3, wherein said different value for unity current gain cutoff frequency than a value for unity current gain cutoff frequency of said otherwise identical bipolar transistor is a lower value.

[c5] 5. The circuit of claim 1, wherein said non-uniform sub-collector region geometry of said first bipolar transistor is selected from the group of geometries consisting of ring geometries having an opening aligned under said emitter of said first bipolar transistor, dual striped geometries having a first stripe located on a first side and a second stripe located on an opposite second side of and away from a plane longitudinally bisecting said emitter of said first bipolar transistor and single striped geometries having a stripe located on one side of and away from a plane longitudinally bisecting said emitter of said first bipolar transistor.

[c6] 6. The circuit of claim 1, wherein said first circuit node is a signal pad and said circuit node is a power rail.

[c7] 7. The circuit of claim 1, wherein said first bipolar transistor is selected from the group of transistors consisting of hetero-junction bipolar transistors, SiGe hetero-junction bipolar transistors, SiGeC hetero-junction bipolar transistors, bipolar homo-junction transistors and bipolar junction transistors.

[c8] 8. The circuit of claim 1, wherein said first bipolar transistor comprises a bulk silicon bipolar transistor or a silicon-on-insulator bipolar transistor.

[c9] 9. The circuit of claim 1, further including
a second bipolar transistor;
a collector of said first bipolar transistor and a collector of said second bipolar transistor coupled to said first circuit node, said first circuit node being a first power rail;
said emitter of said first bipolar transistor and an emitter of said second bipolar transistor coupled to said second circuit node, said second circuit node being a second power rail; and
said emitter of said first bipolar transistor coupled to a base of said second bipolar transistor.

[c10] 10. The circuit of claim 9, wherein said first bipolar transistor has a higher collector to emitter breakdown voltage than said a collector to emitter breakdown of said second bipolar transistor or said first bipolar transistor has a lower collector to emitter breakdown voltage than said collector to emitter breakdown of said second bipolar transistor.

[c11] 11. The circuit of claim 9, wherein second bipolar has a non-uniform subcollector region geometry, said second

bipolar transistor having a different value for collector to emitter breakdown voltage than a value for collector to emitter breakdown voltage of said otherwise identical bipolar transistor.

[c12] 12. The circuit of claim 11, wherein said first bipolar transistor has a lower collector to emitter breakdown voltage than said collector to emitter breakdown of said second bipolar transistor.

[c13] 13. The circuit of claim 1, further including
a second bipolar transistor;
a collector of said second bipolar transistor and a collector of said first bipolar transistor coupled to said first circuit node, said first circuit node being a first power rail;
said emitter of said second bipolar transistor and an emitter of said first bipolar transistor coupled to said second circuit node, said second circuit node being a second power rail; and
said emitter of said second bipolar transistor coupled to a base of said first bipolar transistor.

[c14] 14. The circuit of claim 13, wherein said first bipolar transistor has a higher collector to emitter breakdown voltage than said a collector to emitter breakdown of said second bipolar transistor or said first bipolar tran-

sistor has a lower collector to emitter breakdown voltage than said collector to emitter breakdown of said second bipolar transistor.

[c15] 15. The circuit of claim 9, further including either (a) a resistor coupled between said emitter of said first bipolar transistor and said second power rail, (b) a resistor coupled between said emitter of said second bipolar transistor and said second power rail, or (c) a first resistor coupled between said emitter of said first bipolar transistor and said second power rail and a second resistor coupled between said emitter of said second bipolar transistor and said second power rail.

[c16] 16. The circuit of claim 11, further including either (a) a resistor coupled between said emitter of said first bipolar transistor and said second power rail, (b) a resistor coupled between said emitter of said second bipolar transistor and said second power rail, or (c) a first resistor coupled between said emitter of said first bipolar transistor and said second power rail and a second resistor coupled between said emitter of said second bipolar transistor and said second power rail.

[c17] 17. The circuit of claim 13, further including either (a) a resistor coupled between said emitter of said first bipolar transistor and said second power rail, (b) a resistor

coupled between said emitter of said second bipolar transistor and said second power rail, or (c) a first resistor coupled between said emitter of said first bipolar transistor and said second power rail and a second resistor coupled between said emitter of said second bipolar transistor and said second power rail.

[c18] 18. The circuit of claim 9, further including a varactor network coupled between said collector of said first bipolar transistor and said first power rail.

[c19] 19. The circuit of claim 11, further including a varactor network coupled between said collector of said first bipolar transistor and said first power rail.

[c20] 20. The circuit of claim 13, further including a varactor network coupled between said collector of said second bipolar transistor and said first power rail.

[c21] 21. A method of providing an electrostatic discharge protection to an integrated circuit, comprising:
providing a first bipolar transistor;
coupling said first bipolar transistor between a first circuit node and a second circuit node, said first bipolar transistor having a non-uniform subcollector region geometry; and
selecting said non-uniform subcollector region geometry

in order to tune a collector to emitter breakdown voltage of said first bipolar transistor.

[c22] 22. The method of claim 21, further including selecting said non-uniform subcollector region geometry in order to tune a unity current gain cutoff frequency of said first bipolar transistor.

[c23] 23. The method of claim 21, wherein said non-uniform subcollector region geometry of said first bipolar transistor is selected from the group of geometries consisting of ring geometries having an opening aligned under said emitter of said first bipolar transistor, dual striped geometries having a first stripe located on a first side and a second stripe located on an opposite second side of and away from a plane longitudinally bisecting said emitter of said first bipolar transistor and single striped geometries having a stripe located on one side of and away from a plane longitudinally bisecting said emitter of said first bipolar transistor.

[c24] 24. The method of claim 21, wherein said first bipolar transistor is selected from the group of transistors consisting of hetero-junction bipolar transistors, SiGe hetero-junction bipolar transistors, SiGeC hetero-junction bipolar transistors, bipolar homo-junction transistors and bipolar junction transistors.

[c25] 25. The method of claim 21, wherein said first bipolar transistor comprises a bulk silicon bipolar transistor or a silicon-on-insulator bipolar transistor.

[c26] 26. The method of claim 21, wherein said first circuit node is a signal pad and said circuit node is a power rail.

[c27] 27. The method of claim 21, further including
providing a collector of said first bipolar transistor and a collector of said second bipolar transistor coupled to said first circuit node, said first circuit node being a first power rail;
said emitter of said first bipolar transistor and an emitter of said second bipolar transistor coupled to said second circuit node, said second circuit node being a second power rail; and
said emitter of said first bipolar transistor coupled to a base of said second bipolar transistor.

[c28] 28. The method of claim 27, wherein said first bipolar transistor has a higher collector to emitter breakdown voltage than said a collector to emitter breakdown of said second bipolar transistor or said first bipolar transistor has a lower collector to emitter breakdown voltage than said collector to emitter breakdown of said second bipolar transistor.

[c29] 29. The method of claim 27, wherein second bipolar has a non-uniform subcollector region geometry, said second bipolar transistor having a different value for collector to emitter breakdown voltage than a value for collector to emitter breakdown voltage of said otherwise identical bipolar transistor.

[c30] 30. The method of claim 29, wherein said first bipolar transistor has a lower collector to emitter breakdown voltage than said collector to emitter breakdown of said second bipolar transistor.

[c31] 31. The circuit of claim 21, further including
providing a second bipolar transistor;
providing a collector of said second bipolar transistor and a collector of said first bipolar transistor coupled to said first circuit node, said first circuit node being a first power rail;
said emitter of said second bipolar transistor and an emitter of said first bipolar transistor coupled to said second circuit node, said second circuit node being a second power rail; and
said emitter of said second bipolar transistor coupled to a base of said first bipolar transistor.

[c32] 32. The method of claim 21, wherein said first bipolar

transistor has a higher collector to emitter breakdown voltage than said a collector to emitter breakdown of said second bipolar transistor or said first bipolar transistor has a lower collector to emitter breakdown voltage than said collector to emitter breakdown of said second bipolar transistor.

[c33] 33. The method of claim 27, further including either (a) a resistor coupled between said emitter of said first bipolar transistor and said second power rail, (b) a resistor coupled between said emitter of said second bipolar transistor and said second power rail, or (c) a first resistor coupled between said emitter of said first bipolar transistor and said second power rail and a second resistor coupled between said emitter of said second bipolar transistor and said second power rail.

[c34] 34. The method of claim 29, further including either (a) a resistor coupled between said emitter of said first bipolar transistor and said second power rail, (b) a resistor coupled between said emitter of said second bipolar transistor and said second power rail, or (c) a first resistor coupled between said emitter of said first bipolar transistor and said second power rail and a second resistor coupled between said emitter of said second bipolar transistor and said second power rail.

[c35] 35. The method of claim 31, further including either (a) a resistor coupled between said emitter of said first bipolar transistor and said second power rail, (b) a resistor coupled between said emitter of said second bipolar transistor and said second power rail, or (c) a first resistor coupled between said emitter of said first bipolar transistor and said second power rail and a second resistor coupled between said emitter of said second bipolar transistor and said second power rail.

[c36] 36. The method of claim 27, further including a varactor network coupled between said collector of said first bipolar transistor and said first power rail.

[c37] 37. The method of claim 29, further including a varactor network coupled between said collector of said first bipolar transistor and said first power rail.

[c38] 38. The method of claim 31, further including a varactor network coupled between said collector of said second bipolar transistor and said first power rail.

[c39] 39. A method of designing an electrostatic discharge protection circuit, comprising:
providing a schematic P-cell circuit generator;
providing a hierarchical P-cell layout generator;
providing a graphical unit interface to said schematic P-

cell circuit generator and said hierarchical P-cell layout generator;

accepting a value for a collector to emitter breakdown voltage target for at least a first bipolar transistor of said electrostatic discharge protection circuit;

selecting a non-uniform subcollector region geometry for said first bipolar transistor based on said value of said collector to emitter breakdown voltage target; and

generating a circuit design and a layout for said electrostatic discharge protection circuit, said electrostatic discharge protection circuit containing said first bipolar transistor.

[c40] 40. The method of claim 39, further including displaying a value for a unity current gain cutoff frequency of said first bipolar transistor.